

## WHAT IS CLAIMED IS:

1        1.    A voltage controlled oscillator (VCO) capable of  
2    receiving a  $+V(IN)$  control voltage and a  $-V(IN)$  control voltage and  
3    outputting a VCO output signal having a frequency of oscillation  
4    determined by said  $+V(IN)$  control voltage and said  $-V(IN)$  control  
5    voltage, said VCO comprising:

6            a storage capacitor capable of being charged linearly by  
7    a constant charge current and discharged linearly by a constant  
8    discharge current;

9            a comparator capable of comparing a voltage on said  
10   storage capacitor to an upper threshold voltage and a lower  
11   threshold voltage, wherein an output of said comparator drops to a  
12   negative saturation voltage ( $-V(SAT)$ ) when said storage capacitor  
13   voltage rises above said upper threshold voltage and said  
14   comparator output rises to a positive saturation voltage ( $+V(SAT)$ )  
15   when said storage capacitor voltage drops below said lower  
16   threshold voltage;

17           a constant charge current source capable of injecting  
18   said constant charge current to said storage capacitor when said  
19   comparator output rises to said positive saturation voltage; and

20           a constant discharge current source capable of draining  
21   said constant discharge current from said storage capacitor when

22 said comparator output drops to said negative saturation voltage.

1        2.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 1 wherein said comparator output is coupled to said VCO  
3    output.

1        3.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 2 wherein said constant charge current is determined by said  
3    +V(IN) control voltage.

1        4.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 3 wherein said constant discharge current is determined by  
3    said -V(IN) control voltage.

1        5.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 4 wherein said constant charge current source comprises a  
3    PNP-type bipolar junction transistor having a base coupled to said  
4    +V(IN) control voltage, an emitter coupled to said comparator  
5    output via a load resistor, and a collector coupled to said storage  
6    capacitor.

1        6.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 5 wherein said constant charge current source comprises a  
3    NPN-type bipolar junction transistor having a base coupled to said  
4    -V(IN) control voltage, an emitter coupled to said comparator  
5    output via said load resistor, and a collector coupled to said  
6    storage capacitor.

1        7.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 6 wherein said comparator comprises: 1) an operational  
3    amplifier having an inverting input coupled to said storage  
4    capacitor; 2) a first resistor (R1) having a first terminal coupled  
5    to ground and a second terminal coupled to a non-inverting input of  
6    said operational amplifier; and 3) a second resistor (R2) having a  
7    first terminal coupled to an output of said operational amplifier  
8    and a second terminal coupled to said non-inverting input of said  
9    operational amplifier, wherein said operational amplifier output  
10   comprises said comparator output.

1        8.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 7 wherein said upper threshold voltage is determined by the  
3    product:  $[(R1)/(R1+R2)][+V(SAT)]$ .

1        9.    The voltage controlled oscillator (VCO) as set forth in  
2    Claim 7 wherein said lower threshold voltage is determined by the  
3    product:  $[(R1)/(R1+R2)] [-V(SAT)]$ .

1        10.   The voltage controlled oscillator (VCO) as set forth in  
2    Claim 6 wherein said constant charge current is determined by a  
3    difference between said positive saturation voltage and said +V(IN)  
4    control voltage and constant discharge current is determined by a  
5    difference between said negative saturation voltage and said -V(IN)  
6    control voltage.

1        11. A processing system comprising:

2            a clocked circuit capable of operating at very low  
3 frequency using an external clock signal; and

4            a phase-locked loop (PLL) coupled to said clocked circuit  
5 capable of supplying said external clock signal with high linearity  
6 at very low frequency, said PLL comprising:

7            a frequency divider circuit for dividing a frequency  
8 of said external clock signal by N;

9            a phase detector capable of detecting a phase  
10 difference between a frequency divided output of said  
11 frequency divider circuit and an input reference signal and  
12 generating therefrom a phase difference signal;

13           a charge pump and loop filter circuit capable of  
14 converting said phase difference signal to a +V(IN) control  
15 voltage and a -V(IN) control voltage; and

16           a voltage controlled oscillator (VCO) capable of  
17 receiving said +V(IN) control voltage and said -V(IN) control  
18 voltage and outputting a VCO output signal having a frequency  
19 of oscillation determined by said +V(IN) control voltage and  
20 said -V(IN) control voltage, said VCO comprising:

21           a storage capacitor capable of being charged  
22 linearly by a constant charge current and discharged

23 linearly by a constant discharge current;

24 a comparator capable of comparing a voltage on  
25 said storage capacitor to an upper threshold voltage and  
26 a lower threshold voltage, wherein an output of said  
27 comparator drops to a negative saturation voltage ( $-V(\text{SAT})$ ) when said storage capacitor voltage rises above  
28 said upper threshold voltage and said comparator output  
29 rises to a positive saturation voltage ( $+V(\text{SAT})$ ) when  
30 said storage capacitor voltage drops below said lower  
31 threshold voltage;  
32

33 a constant charge current source capable of  
34 injecting said constant charge current to said storage  
35 capacitor when said comparator output rises to said  
36 positive saturation voltage; and

37 a constant discharge current source capable of  
38 draining said constant discharge current from said  
39 storage capacitor when said comparator output drops to  
40 said negative saturation voltage.

1 12. The processing system as set forth in Claim 11 wherein  
2 said comparator output is coupled to said VCO output.

1        13. The processing system as set forth in Claim 12 wherein  
2        said constant charge current is determined by said +V(IN) control  
3        voltage.

1        14. The processing system as set forth in Claim 13 wherein  
2        said constant discharge current is determined by said -V(IN)  
3        control voltage.

1        15. The processing system as set forth in Claim 14 wherein  
2        said constant charge current source comprises a PNP-type bipolar  
3        junction transistor having a base coupled to said +V(IN) control  
4        voltage, an emitter coupled to said comparator output via a load  
5        resistor, and a collector coupled to said storage capacitor.

1        16. The processing system as set forth in Claim 15 wherein  
2        said constant charge current source comprises a NPN-type bipolar  
3        junction transistor having a base coupled to said -V(IN) control  
4        voltage, an emitter coupled to said comparator output via said load  
5        resistor, and a collector coupled to said storage capacitor.

1        17. The processing system as set forth in Claim 16 wherein  
2        said comparator comprises: 1) an operational amplifier having an  
3        inverting input coupled to said storage capacitor; 2) a first  
4        resistor (R1) having a first terminal coupled to ground and a  
5        second terminal coupled to a non-inverting input of said  
6        operational amplifier; and 3) a second resistor (R2) having a first  
7        terminal coupled to an output of said operational amplifier and a  
8        second terminal coupled to said non-inverting input of said  
9        operational amplifier, wherein said operational amplifier output  
10       comprises said comparator output.

1        18. The processing system as set forth in Claim 17 wherein  
2        said upper threshold voltage is determined by the product:  
3         $[(R1)/(R1+R2)][+V(SAT)]$ .

1        19. The processing system as set forth in Claim 17 wherein  
2        said lower threshold voltage is determined by the product:  
3         $[(R1)/(R1+R2)][-V(SAT)]$ .



1        20. The processing system as set forth in Claim 16 wherein  
2        said constant charge current is determined by a difference between  
3        said positive saturation voltage and said  $+V(IN)$  control voltage  
4        and constant discharge current is determined by a difference  
5        between said negative saturation voltage and said  $-V(IN)$  control  
6        voltage.